

Read Me

Table of Contents

1. これは何か？
2. Platform Design の構造

1. これは何か？

Platform Designer で階層構造 (sub-system) を作り、かつ sub-system の配下の複数の Avalon-MM Agent の agent インタフェースを仲介機構 (Avalon-MM Pipeline Bridge) で一つの agent インタフェースにまとめて上位の階層に見せる具体例。

2. Platform Design の構造

U...	Connections	Name	Description	Export	Clock	Base	End	I...	Tags
<input checked="" type="checkbox"/>		clk_0	Clock Source						
		clk_in	Clock Input	clk	exported				
		clk_in_reset	Reset Input	reset					
		clk	Clock Output	clk					
		clk_reset	Reset Output	reset					
<input checked="" type="checkbox"/>		nios2_gen2_0	Nios II Processor						
		clk	Clock Input	clk	clk_0				
		reset	Reset Input	reset	[clk]				
		data_master	Avalon Memory Mapped Master		[clk]				
		instruction_master	Avalon Memory Mapped Master		[clk]				
		irq	Interrupt Receiver		[clk]			IRQ 0	IRQ 31
		debug_reset_request	Reset Output		[clk]				
		debug_mem_slave	Avalon Memory Mapped Slave		[clk]	0x5000	0x57ff		
		custom_instruction_master	Custom Instruction Master		[clk]				
<input checked="" type="checkbox"/>		oc_mem_0	On-Chip Memory (RAM or ROM) Intel...						
		clk1	Clock Input	clk1	clk_0				
		s1	Avalon Memory Mapped Slave		[clk1]	0x2000	0x3fff		
		reset1	Reset Input	reset1	[clk1]				
<input checked="" type="checkbox"/>		jtag_uart_0	JTAG UART Intel FPGA IP						
		clk	Clock Input	clk	clk_0				
		reset	Reset Input	reset	[clk]				
		avalon_jtag_slave	Avalon Memory Mapped Slave		[clk]	0x5808	0x580f		
		irq	Interrupt Sender	irq	[clk]				
<input checked="" type="checkbox"/>		sysid_qsys_0	System ID Peripheral Intel FPGA IP						
		clk	Clock Input	clk	clk_0				
		reset	Reset Input	reset	[clk]				
		control_slave	Avalon Memory Mapped Slave		[clk]	0x5800	0x5807		
<input checked="" type="checkbox"/>		my_sub_sys_0	my_sub_sys						
		clock_bridge_0_in_clk	Clock Input	clock_bridge_0_in_clk	clk_0				
		mm_bridge_0_s0	Avalon Memory Mapped Slave		[clock_bridge_0_in_clk]	0x4800	0x4fff		
		pio_0_external_connection	Conduit	pio_0_external_connection					
		reset_bridge_0_in_reset	Reset Input	reset_bridge_0_in_reset	[clock_bridge_0_in_clk]				

U...	Connec...	Name	Description	Export	Clock	Base	End
<input checked="" type="checkbox"/>		onchip_memory2_0	On-Chip Memory (RAM or ROM) Intel...				
		clk1	Clock Input	clk1	clock_bridge_0_out_clk	0x0000	0x03ff
		s1	Avalon Memory Mapped Slave		[clk1]		
		reset1	Reset Input	reset1	[clk1]		
<input checked="" type="checkbox"/>		pio_0	PIO (Parallel I/O) Intel FPGA IP				
		clk	Clock Input	clk	clock_bridge_0_out_clk	0x0400	0x040f
		reset	Reset Input	reset	[clk]		
		s1	Avalon Memory Mapped Slave		[clk]		
		external_connection	Conduit	external_connection			
<input checked="" type="checkbox"/>		clock_bridge_0	Clock Bridge				
		in_clk	Clock Input	in_clk	clock_bridge_0_in_clk		
		out_clk	Clock Output	out_clk	clock_bridge_0_out_clk		
<input checked="" type="checkbox"/>		reset_bridge_0	Reset Bridge				
		clk	Clock Input	clk	clock_bridge_0_out_clk		
		in_reset	Reset Input	in_reset	reset_bridge_0_in_clk		
		out_reset	Reset Output	out_reset	[clk]		
<input checked="" type="checkbox"/>		mm_bridge_0	Avalon-MM Pipeline Bridge				
		clk	Clock Input	clk	clock_bridge_0_out_clk		
		reset	Reset Input	reset	[clk]		
		s0	Avalon Memory Mapped Slave		[clk]		
		m0	Avalon Memory Mapped Master		[clk]		

Figure 1. top-layer and sub-layer